REMARKS

Claims 2 and 8-27 are all the claims pending in the application.

Applicants respectfully request that the Examiner reconsider the rejections to the claims in light of the discussions below.

Claims 2 and 8-27stand rejected under 35 U.S.C. §112, first paragraph.

Claims 2 and 8-27 stand rejected under 35 U.S.C. §112, second paragraph.

Claims 2 and 8-27 stand rejected under 35 U.S.C. §101.

Applicants respectfully traverse the rejection for the following reasons.

I. The 35 U.S.C. §112, First Paragraph, Rejection

[0001] Claims 2, and 8-27 stand rejected under 35 U.S.C. §112, first paragraph, because the Office Action asserts that the claimed invention is directed to software models of a CPU, an SOC interface and EBIU interfaces that are implemented in a computer system.

[0002] The Office Action states that regarding independent claim 2 and the dependent claims, the specification appears to be directed to software models of a CPU, an SOC interface and EBIU interfaces that are implemented in a computer system.

[0003] Applicants respectfully submit Paragraph [0003] of the Background section of the Specification recites in relevant part, "Hardware verification typically entails the use of software "models" of design logic." Paragraph [0004] of the Background section of the Specification recites in relevant part, "The term 'SOC' [i.e., system-on-a-chip] as used herein refers to combinations of discrete logic blocks, often referred to as 'cores', each performing a different function of group of functions. A SOC integrates a plurality of cores into a single silicon device, thereby providing a wide range of functions in a highly compact form." Paragraph [0005] of the Background section of the Specification recites in relevant part, "In its developmental stage, a core is typically embodied as a simulatable HDL model … . A core may be in the form of a netlist … ." Paragraph [0006] of the Background section of the Specification recites in relevant part, "Verification of a SOC presents challenges because of the number of cores and the complexity of interactions involved, both between the cores internally to the SOC, and between

the SOC and external logic." Paragraph [0007] of the Background section of the Specification recites in relevant part, "According to one standard technique, already-verified models are used to test other models. The electronic design automation (EDA) industry has reached a level of sophistication wherein vendors offer standardized models for use in verification of other models still in development." Paragraph [0008] of the Background section of the Specification recites in relevant part, "However, there are disadvantages associated with using standardized models."

[0004] Applicants now recite the first paragraph, i.e., [0010], of the Summary of the Invention section, "In view of the foregoing and other problems, disadvantages, and drawbacks of conventional verification test benches, the present invention has been devised, and it is an object of the present invention to provide a structure that attaches an external model to a SOC interface and to an external bus interface unit."

[0005] Applicants respectfully submit that paragraphs [0002]-[0009] describe the related art, which may be paraphrased as follows: Hardware verification of integrated circuits typically entails use of software models for logic blocks. A system-on-a chip (SOC) comprises a number of logic blocks, also called "cores", which are integrated into a single silicon device. Conventional techniques of verification of the logic blocks of an SOC may use HDL models or netlists. However, hardware verification of an SOC presents challenges because of the complexity of interaction between logic blocks of the SOC and between the SOC and external logic devices. Standardized software models used for models of the logic blocks, still in development, have disadvantages.

[0006] In other words, according to the related art section of the Specification, hardware verification by software models of the logic blocks, comprising an SOC, have disadvantages.

[0007] Therefore, as recited in paragraph [0010] of the Summary of the Invention, another approach to overcoming the disadvantages of conventional software modeling of logic blocks for hardware verification of an SOC are described, i.e., a structure (i.e., hardware) that attaches an external model (i.e., hardware) to a SOC interface (i.e., hardware) and to an external bus interface unit (i.e., hardware)."

[0008] As is known to those in the art of chip design and verification, verification by software has its disadvantages. In particular, race conditions are difficult to resolve through

software verification. For example, imagine a 2-input NAND gate within a chip to be verified. The first input to the NAND gate derives from a logic block comprising 15 gates, whereas the second input to the NAND gate derives from a logic block comprising but 10 gates. The first input signal will arrive at the NAND before the second input (assuming length and impedances of the input lines are approximately equal). That is, the proper output for the NAND gate is not when the first input arrives but is delayed by the timing of the second input, and whatever delays there are associated with the NAND gate itself. In the floor planning of an SOC, unanticipated delays between logic blocks (even when CLOCKed) can lead to errors from expected functional outputs. Thus, the present invention uses a hardware SOC to test itself, by running test patterns on itself, sending the results to an external verification test bench including a verification interface model, which also receives signals from the SOC interface, to verify the hardware logic of the hardware SOC.

[0009] The Office Action especially refers to paragraph [0025] of the Specification, which refers to Fig. 2, of the application; however, all of the pending claims, are clearly shown in Fig. 1 of the application, not Fig. 2.

[0010] The Office Action also states that the specification appears to be directed to verification of HDL models of a SOC (*see especially paragraphs [0001]-[0008]*), and does not appear to intend to support a system with a physical CPU, a physical SOC interface, and physical EBIU interfaces. Especially see the specification paragraphs [0004]-[0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist.

[0011] For the identical reasons outlined above, with respect to the Office Action's assertion that the specification appears to be directed to a software invention that is implemented in a computer, Applicants respectfully argue that paragraphs [0002]-[0008] describe the convention related art and not the present invention.

[0012] The present invention is clearly described in paragraphs [0019]-[0024] and [0026], the elements of which are shown in Fig. 1 of the specification. As a convenience to the Examiner, Applicants provide the following annotated independent claims, in which the annotations refer to the present invention's features in the text, indicated by paragraph number

and line numbers within each paragraph, and the figures, indicated by Figure number and element number, of the Specification.

Independent claim 2

[0013] A system for verifying integrated circuit logic of a system-on-a-chip (SOC) design, said system comprising:

an SOC ([0022], lines 5, 6; [0023], line 10, 13; [0024], lines 2, 6; Fig. 1, 100) comprising:

a master central processing unit (CPU) ([0022], lines 4, 5, 7; Fig. 1, 130) that produces a first set of signals and a second set of signals for verifying said integrated circuit logic in response to running a verification case;

an SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) that receives said second set of signals; and

a first external bus interface unit (EBIU) ([0020], line 1; [0023], line 10; Fig. 1, 205) that is slaved to said master CPU ([0022], lines 4, 5, 7; Fig. 1, 130) and receives said first set of signals; and

a verification test bench ([0019], line 4; [0020], line 2; [0022], line 9; Fig. 1, 300) that is external to said SOC ([0022], lines 5, 6; [0023], line 10, 13; [0024], lines 2, 6; Fig. 1, 100), said verification test bench ([0019], line 4; [0020], line 2; [0022], line 9; Fig. 1, 300) comprising:

a verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210) connected to said SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101); and

a second EBIU ([0019], lines 2, 5; [0020], line 1; [0022], line 3; [0023], line 10; Fig. 1, 200) connected to said first EBIU ([0020], line 1; [0023], line 10; Fig. 1, 205) and to said verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210);

wherein said first set of signals received by said second EBIU ([0019], lines 2, 5; [0020], line 1; [0022], line 3; [0023], line 10; Fig. 1, 200) is inputted to said verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210) and said verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210) outputs data for said verification case to said SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101); and

wherein said verification case checks for correctness of said outputted data from said verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210) to said SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) by said second set of signals and records a verification case status.

Independent claim 8

[0014] A system for verifying integrated circuit logic of a system-on-a-chip (SOC), said system comprising:

an SOC ([0022], lines 5, 6; [0023], line 10, 13; [0024], lines 2, 6; Fig. 1, 100) comprising:

a master central processing unit (CPU) ([0022], lines 4, 5, 7; Fig. 1, 130) that produces a first set of signals and a second set of signals for verifying said integrated circuit logic in response to signals produced by running a verification case;

an SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) that receives said second set of signals, said SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) being connected to said master CPU ([0022], lines 4, 5, 7; Fig. 1, 130) by a first internal bus; and

a first external bus interface unit (EBIU) ([0020], line 1; [0023], line 10; Fig. 1, 205) that is slaved and connected to said master CPU ([0022], lines 4, 5, 7; Fig. 1, 130) by a second internal bus ([0022], line 5; Fig. 1, 131); and

a verification test bench ([0019], line 4; [0020], line 2; [0022], line 9; Fig. 1, 300) that is external to said SOC ([0022], lines 5, 6; [0023], line 10, 13; [0024], lines 2, 6; Fig. 1, 100), said verification test bench ([0019], line 4; [0020], line 2; [0022], line 9; Fig. 1, 300) comprising:

a verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210) connected to said SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) by a second external bus (Fig. 1, DATA); and

a second EBIU ([0019], lines 2, 5; [0020], line 1; [0022], line 3; [0023], line 10; Fig. 1, 200) connected to said first EBIU ([0020], line 1; [0023], line 10; Fig. 1, 205) by a first external bus (Fig. 1, 206) and to said verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210) by a third internal bus (Fig. 1, 201);

wherein said first set of signals received by said second EBIU ([0019], lines 2, 5; [0020], line 1; [0022], line 3; [0023], line 10; Fig. 1, 200) is inputted to said verification interface model via ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210) said third internal bus (Fig. 1, 201) and said verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210) outputs data for said verification case to said SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) via said data bus (Fig.1, DATA); and

wherein said verification case checks for correctness of said outputted data from said verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210) to said SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) by said second set of signals via said first internal bus and records a verification case status.

Independent claim 15

[0015] A system for verifying integrated circuit logic of a system-on-a-chip (SOC), said system comprising:

an SOC ([0022], lines 5, 6; [0023], line 10, 13; [0024], lines 2, 6; Fig. 1, 100) comprising:

a master central processing unit (CPU) ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) that produces a first set of signals and a second set of signals for verifying said integrated circuit logic in response to signals produced by running a verification case;

an SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) that receives said second set of signals, said SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) being connected to said master CPU ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) by a first internal bus; and

a first external bus interface unit (EBIU) ([0020], line 1; [0023], line 10; Fig. 1, 205) that is slaved and connected to said master CPU ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) by a second internal bus ([0022], line 5; Fig. 1, 131); and

a verification test bench ([0019], line 4; [0020], line 2; [0022], line 9; Fig. 1, 300) that is external to said SOC ([0022], lines 5, 6; [0023], line 10, 13; [0024], lines 2, 6; Fig. 1, 100), said verification test bench ([0019], line 4; [0020], line 2; [0022], line 9; Fig. 1, 300) comprising:

a verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210) connected to said SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) by a second external bus ([0022], line 5; Fig. 1, 131); and

a second EBIU ([0019], lines 2, 5; [0020], line 1; [0022], line 3; [0023], line 10; Fig. 1, 200) connected to said first EBIU ([0020], line 1; [0023], line 10; Fig. 1, 205) by a first external bus (Fig. 1, 206) and to said verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210) by a third internal bus (Fig. 1, 201);

wherein said second EBIU ([0019], lines 2, 5; [0020], line 1; [0022], line 3; [0023], line 10; Fig. 1, 200) and said first EBIU ([0020], line 1; [0023], line 10; Fig. 1, 205)

are mastered by said master CPU ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) of said SOC ([0022], lines 5, 6; [0023], line 10, 13; [0024], lines 2, 6; Fig. 1, 100), such that, said SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) and said verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210) receive said first set of signals and said second set of signals, respectively, as inputs based on the running of said verification case by said master CPU ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101); and

wherein said verification case checks for correctness of outputted data from said verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210) to said SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) by said second set of signals and records a verification status.

Independent claim 21

[0016] A method for verifying integrated circuit logic of a system-on-a-chip (SOC), said method comprising:

producing a first set of signals and a second set of signals by a master central processing unit (CPU) ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) of an SOC ([0022], lines 5, 6; [0023], line 10, 13; [0024], lines 2, 6; Fig. 1, 100), which includes said integrated circuit logic, in response to running a verification case on said master CPU ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101);

slaving an SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101), which receives said second set of signals, and a first external bus interface unit (EBIU) ([0020], line 1; [0023], line 10; Fig. 1, 205) of said SOC ([0022], lines 5, 6; [0023], line 10, 13; [0024], lines 2, 6; Fig. 1, 100), which receives said first set of signals, to said master CPU ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5,

6, 11; Fig. 1, 101) of said SOC ([0022], lines 5, 6; [0023], line 10, 13; [0024], lines 2, 6; Fig. 1, 100);

connecting said SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) to an external verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210), which is external to said SOC ([0022], lines 5, 6; [0023], line 10, 13; [0024], lines 2, 6; Fig. 1, 100);

connecting said first EBIU ([0020], line 1; [0023], line 10; Fig. 1, 205) to a second EBIU ([0019], lines 2, 5; [0020], line 1; [0022], line 3; [0023], line 10; Fig. 1, 200), which is external to said SOC ([0022], lines 5, 6; [0023], line 10, 13; [0024], lines 2, 6; Fig. 1, 100), said second EBIU ([0019], lines 2, 5; [0020], line 1; [0022], line 3; [0023], line 10; Fig. 1, 200) being connected to said external verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210);

inputting said first set of signals, received by said second EBIU ([0019], lines 2, 5; [0020], line 1; [0022], line 3; [0023], line 10; Fig. 1, 200), into said verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210);

inputting said second set of signals, received by said SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101); and

verifying said verification case by checking for correctness of said outputted data from said verification interface model ([0019], lines 2, 6; [0022], lines 1, 9; [0023], lines 1, 5, 9, 11, 12; [0024], lines 3, 4, 7; [0026], lines 6, 10; Fig. 1, 210) to said SOC interface ([0022], line 2, 7; [0023], lines 2, 3, 5, 12; [0024], lines 3, 4, 6; [0026], lines 5, 6, 11; Fig. 1, 101) by said second set of signals and recording a verification case status.

[0017] For at least the reasons outlined above, Applicants respectfully submit that previously presented, independent claims 2, 8, 15, and 21, and dependent claims 9-14, 16-20, and 22-27 fulfill the statutory requirements of 35 U.S.C. §112, first paragraph. Withdrawal of the rejection of claims 2 and 8-27 under 35 U.S.C. §112, first paragraph, is respectfully solicited.

II. The 35 U.S.C. §112, Second Paragraph, Rejection

[0018] The Office Action states that the specification appears to be directed to a software invention that is implemented in a computer. Especially see the specification paragraphs [0004]-[0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist. Currently, the elements of the claim appear to have an interpretation as either physical hardware or a software model.

[0019] Applicants respectfully submit Paragraph [0003] of the Background section of the Specification recites in relevant part, "Hardware verification typically entails the use of software "models" of design logic." Paragraph [0004] of the Background section of the Specification recites in relevant part, "The term 'SOC' [i.e., system-on-a-chip] as used herein refers to combinations of discrete logic blocks, often referred to as 'cores', each performing a different function of group of functions. A SOC integrates a plurality of cores into a single silicon device, thereby providing a wide range of functions in a highly compact form." Paragraph [0005] of the Background section of the Specification recites in relevant part, "In its developmental stage, a core is typically embodied as a simulatable HDL model ... . A core may be in the form of a netlist ... ." Paragraph [0006] of the Background section of the Specification recites in relevant part, "Verification of a SOC presents challenges because of the number of cores and the complexity of interactions involved, both between the cores internally to the SOC, and between the SOC and external logic." Paragraph [0007] of the Background section of the Specification recites in relevant part, "According to one standard technique, already-verified models are used to test other models. The electronic design automation (EDA) industry has reached a level of sophistication wherein vendors offer standardized models for use in verification of other models still in development." Paragraph [0008] of the Background section of the Specification recites in relevant part, "However, there are disadvantages associated with using standardized models."

[0020] Applicants now recite the first paragraph, i.e., [0010], of the Summary of the Invention section, "In view of the foregoing and other problems, disadvantages, and drawbacks of conventional verification test benches, the present invention has been devised, and it is an

object of the present invention to provide a structure that attaches an external model to a SOC interface and to an external bus interface unit."

[0021] Applicants respectfully submit that paragraphs [0002]-[0009] describe the related art, which may be paraphrased as follows: Hardware verification of integrated circuits typically entails use of software models for logic blocks. A system-on-a chip (SOC) comprises a number of logic blocks, also called "cores", which are integrated into a single silicon device. Conventional techniques of verification of the logic blocks of an SOC may use HDL models or netlists. However, hardware verification of an SOC presents challenges because of the complexity of interaction between logic blocks of the SOC and between the SOC and external logic devices. Standardized software models used for models of the logic blocks, still in development, have disadvantages.

[0022] In other words, according to the related art section of the Specification, hardware verification by software models of the logic blocks, comprising an SOC, have disadvantages.

[0023] Therefore, as recited in paragraph [0010] of the Summary of the Invention, another approach to overcoming the disadvantages of conventional software modeling of logic blocks for hardware verification of an SOC are described, i.e., a structure (i.e., hardware) that attaches an external model (i.e., hardware) to a SOC interface (i.e., hardware) and to an external bus interface unit (i.e., hardware)."

[0024] As is known to those in the art of chip design and verification, verification by software has its disadvantages. In particular, race conditions are difficult to resolve through software verification. For example, imagine a 2-input NAND gate within a chip to be verified. The first input to the NAND gate derives from a logic block comprising 15 gates, whereas the second input to the NAND gate derives from a logic block comprising but 10 gates. The first input signal will arrive at the NAND before the second input (assuming length and impedances of the input lines are approximately equal). That is, the proper output for the NAND gate is not when the first input arrives but is delayed by the timing of the second input, and whatever delays there are associated with the NAND gate itself. In the floor planning of an SOC, unanticipated delays between logic blocks (even when CLOCKed) can lead to errors from expected functional outputs. Thus, the present invention uses a hardware SOC to test itself, by running test patterns

on itself, sending the results to an external verification test bench including a verification interface model, which also receives signals from the SOC interface, to verify the hardware logic of the hardware SOC.

[0025] The Office Action especially refers to paragraph [0025] of the Specification, which refers to Fig. 2, of the application; however, all of the pending claims, are clearly shown in Fig. 1 of the application, not Fig. 2.

[0026] The Office Action also states that the specification appears to be directed to verification of HDL models of a SOC (*see especially paragraphs [0001]-[0008]*), and does not appear to intend to support a system with a physical CPU, a physical SOC interface, and physical EBIU interfaces. Especially see the specification paragraphs [0004]-[0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist.

[0027] For the identical reasons outlined above, with respect to the Office Action's assertion that the specification appears to be directed to a software invention that is implemented in a computer, Applicants respectfully argue that paragraphs [0002]-[0008] describe the convention related art and not the present invention.

[0028] The present invention is clearly described in paragraphs [0019]-[0024] and [0026], the elements of which are shown in Fig. 1 of the specification.

[0029] For at least the reasons outlined above, Applicants respectfully submit that previously presented, independent claims 2, 8, 15, and 21, and dependent claims 9-14, 16-20, and 22-27 fulfill the statutory requirements of 35 U.S.C. §112, second paragraph. Withdrawal of the rejection of claims 2 and 8-27 under 35 U.S.C. §112, second paragraph, is respectfully solicited.

III. The 35 U.S.C. §101 Rejection

[0030] The Office Action states that the specification appears to be directed to a software invention that is implemented in a computer. Especially see the specification paragraphs [0004]-[0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL

model, and may be in the form of a netlist. Currently, the elements of the claim appear to have an interpretation as either physical hardware or a software model.

[0031] Applicants respectfully submit Paragraph [0003] of the Background section of the Specification recites in relevant part, "Hardware verification typically entails the use of software "models" of design logic." Paragraph [0004] of the Background section of the Specification recites in relevant part, "The term 'SOC' [i.e., system-on-a-chip] as used herein refers to combinations of discrete logic blocks, often referred to as 'cores', each performing a different function of group of functions. A SOC integrates a plurality of cores into a single silicon device, thereby providing a wide range of functions in a highly compact form." Paragraph [0005] of the Background section of the Specification recites in relevant part, "In its developmental stage, a core is typically embodied as a simulatable HDL model ... . A core may be in the form of a netlist ... ." Paragraph [0006] of the Background section of the Specification recites in relevant part, "Verification of a SOC presents challenges because of the number of cores and the complexity of interactions involved, both between the cores internally to the SOC, and between the SOC and external logic." Paragraph [0007] of the Background section of the Specification recites in relevant part, "According to one standard technique, already-verified models are used to test other models. The electronic design automation (EDA) industry has reached a level of sophistication wherein vendors offer standardized models for use in verification of other models still in development." Paragraph [0008] of the Background section of the Specification recites in relevant part, "However, there are disadvantages associated with using standardized models."

[0032] Applicants now recite the first paragraph, i.e., [0010], of the Summary of the Invention section, "In view of the foregoing and other problems, disadvantages, and drawbacks of conventional verification test benches, the present invention has been devised, and it is an object of the present invention to provide a structure that attaches an external model to a SOC interface and to an external bus interface unit."

[0033] Applicants respectfully submit that paragraphs [0002]-[0009] describe the related art, which may be paraphrased as follows: Hardware verification of integrated circuits typically entails use of software models for logic blocks. A system-on-a chip (SOC) comprises a number of logic blocks, also called "cores", which are integrated into a single silicon device.

Conventional techniques of verification of the logic blocks of an SOC may use HDL models or netlists. However, hardware verification of an SOC presents challenges because of the complexity of interaction between logic blocks of the SOC and between the SOC and external logic devices. Standardized software models used for models of the logic blocks, still in development, have disadvantages.

[0034] In other words, according to the related art section of the Specification, hardware verification by software models of the logic blocks, comprising an SOC, have disadvantages.

[0035] Therefore, as recited in paragraph [0010] of the Summary of the Invention, another approach to overcoming the disadvantages of conventional software modeling of logic blocks for hardware verification of an SOC are described, i.e., a structure (i.e., hardware) that attaches an external model (i.e., hardware) to a SOC interface (i.e., hardware) and to an external bus interface unit (i.e., hardware)."

[0036] As is known to those in the art of chip design and verification, verification by software has its disadvantages. In particular, race conditions are difficult to resolve through software verification. For example, imagine a 2-input NAND gate within a chip to be verified. The first input to the NAND gate derives from a logic block comprising 15 gates, whereas the second input to the NAND gate derives from a logic block comprising but 10 gates. The first input signal will arrive at the NAND before the second input (assuming length and impedances of the input lines are approximately equal). That is, the proper output for the NAND gate is not when the first input arrives but is delayed by the timing of the second input, and whatever delays there are associated with the NAND gate itself. In the floor planning of an SOC, unanticipated delays between logic blocks (even when CLOCKed) can lead to errors from expected functional outputs. Thus, the present invention uses a hardware SOC to test itself, by running test patterns on itself, sending the results to an external verification test bench including a verification interface model, which also receives signals from the SOC interface, to verify the hardware logic of the hardware SOC.

[0037] The Office Action especially refers to paragraph [0025] of the Specification, which refers to Fig. 2, of the application; however, all of the pending claims, are clearly shown in Fig. 1 of the application, not Fig. 2.

[0038] The Office Action also states that the specification appears to be directed to verification of HDL models of a SOC (*see especially paragraphs [0001]-[0008]*), and does not appear to intend to support a system with a physical CPU, a physical SOC interface, and physical EBIU interfaces. Especially see the specification paragraphs [0004]-[0005] that appear to define an SOC as cores, and a core is embodied as a simulatable HDL model, and may be in the form of a netlist.

[0039] For the identical reasons outlined above, with respect to the Office Action's assertion that the specification appears to be directed to a software invention that is implemented in a computer, Applicants respectfully argue that paragraphs [0002]-[0008] describe the convention related art and not the present invention.

[0040] The present invention is clearly described in paragraphs [0019]-[0024] and [0026], the elements of which are shown in Fig. 1 of the specification.

[0041] For at least the reasons outlined above, Applicants respectfully submit that previously presented, independent claims 2, 8, 15, and 21, and dependent claims 9-14, 16-20, and 22-27 fulfill the statutory requirements of 35 U.S.C. §101. Withdrawal of the rejection of claims 2 and 8-27 under 35 U.S.C. §101 is respectfully solicited.

IV. Formal Matters and Conclusion

Claims 2 and 8-27 are pending in the application.

For at least the reasons outlined above, Applicants respectfully submit that claims 2 and 8-27 fulfill the statutory requirements of 35 U.S.C. §112, first and second paragraphs, and 35 U.S.C. §101.

In view of the foregoing, Applicants submit that claims 2 and 8-27, all the claims presently pending in the application, are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest time possible.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0456.

Respectfully submitted,

Dated: February 17, 2009

/Peter A. Balnave/
Peter A. Balnave, Ph.D.
Registration No. 46,199

Gibb I.P. Law Firm, LLC
2568-A Riva Road, Suite 304
Annapolis, MD 21401
Voice: (410) 573-5255
Fax: (301) 261-8825
Email: Balnave@gibbiplaw.com
Customer Number: 29154